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EXAMINER	
DILLON, SAMUEL A	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,645	LIOU, MING-SHI	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-17 and 19-33* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Examiner acknowledges the applicant's submission of the amendment dated June 29, 2006. Per the amendment, Claims 1-13 have been cancelled, Claims 14 and 17-18 have been amended and Claims 20-33 have been added.

2. The instant application having Application No. 10/707,645 has a total of 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

I. ACKNOWLEDGEMENT OF INFORMATION DISCLOSURE STATEMENT

3. The information disclosure statement (IDS) submitted on July 17, 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

4. As required by M.P.E.P. ' 609 (C), the applicant's submission of the Information Disclosure Statement dated July 17, 2006 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. ' 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

5. In response to the amendment, the objections to the drawings, specification and claims as stated in the previous action are withdrawn.

6. In response to the amendment, the 35 U.S.C. 112 rejection of Claim 18 as stated in the previous action is withdrawn.

7. Applicant's arguments with respect to the 35 U.S.C. 103(a) rejection of Claim 18 have been fully considered and are **persuasive**. The rejection of Claim 18 has been withdrawn.

8. Applicant's arguments with respect to the 35 U.S.C. 103(a) rejection of Claims 14-17 have been fully considered but are **not persuasive**.

9. The Applicant contends *(page 13 lines 10-16)* that the combination of references does not disclose constructing the codes according to the memory size.

Koos and Schmisseur disclose a memory system *(Koos, column 1 lines 13-44)* that uses a prefix address register to keep track of the common address shared by all the memory locations inside a specific memory board *(Schmisseur, column 5 lines 35-60)*. Koos and Schmisseur do not disclose how the common addresses would be assigned, but do disclose that sections have different sizes and that the common address length is based on the number of locations addressable in the section *(Schmisseur, column 4 lines 51-67)*.

Hirschberg uses an algorithm *("Shannon-Fano Coding", section 3.1)* to assign bit masks to weighted elements such that an element with the highest weight receives the shortest bit mask. It has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for

rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

In this case, a set of weighted elements is analogous to a set of sized elements, in that both are sets of elements having a unit of measure. While Hirschberg does not expressly disclose using size as a measure, as a generalized mathematical algorithm the Shannon-Fano coding applies to any set capable of being measured in the mathematical sense. The Applicant is directed to the included reference from Wikipedia *("Measure (mathematics)")* for more information.

Accordingly, the Examiner respectfully asserts that a person having ordinary skill in the art would have found an algorithm accepting weighted elements and returning minimal bit-masks to be reasonably pertinent to the problem of assigning bit-masks to sized elements.

10. Additionally, the Applicant contends that Schmisseur et al. does not teach the bit-pattern as it is described in the instant application, and also does not teach that the given address is compared with the bit-pattern. The Examiner notes that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, Koos discloses a comparison unit that matches if an address is inside a range *(Koos, figure 3)*, and Schmisseur discloses that instead if you use a bit-mask all the comparator would need to do is compare the upper bits to determine a

match *(Schmisseur, column 4 lines 55-59)*. The Applicant is directed to the 35 U.S.C. 103 rejection of Claim 14 below.

11. Applicant's arguments with respect to the double patenting rejections of the claims against copending application 10/708,103 have been fully considered but are **not persuasive**. Though independent claim 12 of the copending application has been amended and considerably narrowed, several additional claims were added to both applications that are still unpatentable in view of each other.

Please see the double patenting rejection below for more information.

IV. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC ' 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. **Claims 19-33** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claims 19 and 28 recite the limitation *"the common rules of the bit"*. It is unclear what this limitation is referring to and what the breadth of the claim might be. For the purposes of further examination, the Examiner will interpret the limitation as reading *"obtaining at least one bit-pattern of each section according to the common bits of the section addresses"*.

15. Claim 28 recites the limitation *"wherein if the memory size of a first section is* ***substantially*** *equal to a second section, the addresses of the first section and* ***the section*** *are swappable".*

The term *"substantially"* is a relative term that renders the claim indefinite. The term is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Additionally, the claim refers to *"the section"*, but before discloses *"a first section"* and *"a second section"*. Subsequently it is unclear what section *"the section"* is referring.

For the purposes of further examination, the Examiner will interpret the claim as reading *"wherein if the memory size of a first section is ~~substantially~~ equal to a second section, the addresses of the first section and the second section are swappable".*

16. Claims 20-27 and 29-33 are rejected by virtue of their dependence.

Claim Rejections – 35 USC ' 101

17. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

18. **Claims 19-33** are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter. The claims appear to disclose methods that do not transform an article or physical object to a different state or thing and do not produce a tangible result.

To direct the claimed inventions to statutory subject matter, the claims must be amended to include performing a physical transformation that produces a tangible result, such as storing the corresponding address, the single bit-pattern or the result of the determination in a memory. The Examiner notes that the same problem occurred in cancelled Claims 1-13 and they were rejected under the same rationale.

VII. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102 - Patterson

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. **Claims 14-15, 19, 24-25, 28 and 31-32** are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson et al. *("Computer Organization & Design")*.

21. As per **Claims 14, 19 and 28**, but more specifically to Claim 14, Patterson discloses a control circuit *(figure B.23)* of memory address decoding for determining whether a given address is located in one of a plurality of sections *(cell, Figure B.23 description line 3)*, each section having at least one memory unit and each memory unit having a unique corresponding address *(a unit is a pair of D latches, figure B.23)*, the corresponding address using the binary system *(inherently implied with having two wire input lines leading into standard logic elements, figure B.23)*, the control circuit comprising:

an access module for receiving the given address *(connection of address line to 2-to-4 decoder, figure B.23)*;

a sorting module *(2-to-4 decoder, figure B.23)* for making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size *(interpreted as claiming that the sorting module forces the circuit to satisfy the invariant that a section of greater size than another has a smaller corresponding address, and as each section is of equal size the 2-to-4 decoder causes the circuit to satisfy that invariant, figure B.23)*, and if the size of a first section is equal to the size of a second section, the first and the second sections are capable of being swapped *(any of the identical D-latch pairs could be switched and the circuit would be functionally equivalent, figure B.23)*; and

a comparing module *(the 2-to-4 decoder inherently implies that its output on the 4 side is the result of the line being selected by the input, the circuitry that determines which output line is selected based on the address fulfills this limitation, figure B.23)* for building a bit-pattern for each section based on its corresponding addresses *(a binary address of 00 will cause the top two D-latches to output, binary 10 will cause the D-latches second from the bottom to output, figure B.23)* and sending a plurality of comparison signals *(each output 0-3 on the 2-to-4 decoder, figure B.23)* after comparing the given address with those of each bit-pattern.

22. As per **Claim 15**, Patterson discloses the control circuit of Claim 14 further

comprising a logic module responsible for receiving the comparison signals and sending a decoding result to determine the given address is located in one of the sections *(enable functionality of each D-latch, figure B.23)*.

23. As per **Claims 24 and 31**, but more specifically to Claim 24, Patterson discloses the method of Claim 18 wherein

the bit-pattern is obtained by all common bits of the address in each section *(the entirety of the two bit address is common per cell, figure B.23)*.

24. As per **Claims 25 and 32**, but more specifically to Claim 25, Patterson discloses the method of Claim 19 wherein

the bit-pattern is obtained by partial common bits of the address in each section *(as the entirety of the two bit address is common per cell, the address of each cell is determined by both common bits as well as by each individual bit, such that the address of the cell can be said to be determined by each of the two partial common bits, figure B.23)*.

Claim Rejections - 35 USC ' 103 – Koos, Schmisseur and Hirscberg

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. **Claims 14-17, 19-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Koos *(US Patent Number 4,400,794)* in view of Schmisseur et al. *(US Patent Number 6,128,718)* and Hirschberg *("Data Compression")*.

27. As per **Claim 19**, Koos discloses

a memory address decoding method of determining an objective section *(memory boards, column 1 line 13)* of a given address *(memory address location, column 1 line 22)* in a memory, wherein the memory is formed by at least one section with at least one memory unit, the method comprising: determining the objective section of the given address *(column 3 lines 20-62)*.

Koos does not disclose obtaining at least one bit-pattern of each section according to the common rules of the bit of the addresses; and comparing the given address with each bit-pattern

Schmisseur discloses

obtaining at least one bit-pattern of each section according to the common rules of the bit of the addresses *(column 4 lines 55-59)*; and

comparing the given address with each bit-pattern *(additional addressing bits, column 4 lines 55-65)*.

Koos and Schmisseur are analogous art in that they both deal with memory mapping and addressing. At the time of the invention it would have been obvious to use Schmisseur's base address register as the means Koos uses to describe a memory's size and start address.

The motivation for doing so would have been that Schmisseur's register provides a proper response to address space queries by host processors that use procedures such as the one defined by the PCI Specification *(Schmisseur, column 8 lines 40-43)*.

Therefore it would have been obvious to combine the system of Koos with Schmisseur's base address register for the benefit of responding correctly to PCI conforming devices.

Koos and Schmisseur disclose using a prefix address register to keep track of the common address shared by all the memory locations inside a specific memory board *(Schmisseur, column 5 lines 35-60)*.

Koos and Schmisseur do not disclose assigning an address to each memory unit according to the memory size of the section *(this limitation is interpreted as not requiring that there be a section with a greater size than another section, but rather that if there does exist a section with greater size than another section, then the section with a greater size has it's corresponding address be made smaller than the section it is greater than)*. Schmisseur additionally does not disclose how the prefix addresses are assigned.

Hirschberg discloses assigning prefix codes to a collection of weighted elements by sorting them in decreasing weighted order *(Hirschberg, section 3.1)*.

Accordingly, Hirschberg discloses

> making the corresponding address in a section with greater size smaller than the corresponding address in a section with smaller size *(Hirschberg, section 3.1 lines 1-2)*.

Koos, Schmisseur and Hirschberg are analogous art in that Koos and Schmisseur assign prefix addresses to a plurality of differently sized memories, and Hirschberg teaches an optimal way of assigning prefix codes to a plurality of weighted elements *(Hirschberg, "Shannon-Fano Coding", section 3.1)*.

At the time of the invention it would have been obvious to one with ordinary skill in the art to modify the memory mapping system taught by Koos and Schmisseur to assign the prefix codes using the Shannon-Fano algorithm, as taught by Hirschberg.

The motivation for doing so would have been that Koos discloses wanting to use the least number of significant bits during calculation *(Koos, column 2 lines 64-66)*, and assigning the prefix codes using the Shannon-Fano algorithm technique yields minimal prefix codes for each element *(Hirschberg, section 3.1, lines 6-7)*.

Therefore, it would have been obvious to assign the prefixes of Koos and Schmisseur using the Shannon-Fano algorithm as taught by Hirschberg for the benefit of yielding minimal prefix codes, to obtain the invention of Claim 19.

The Examiner notes that Claim 27 discloses the additional limitation that if the memory size of a first section is substantially equal to a second section, the addresses of the first section and the section are swappable *(Hirschberg discloses the elements being listed in order of non-increasing probability, which inherently does not render incapable the possibility of elements with the same probability being in any order, section 3.1, lines 1-2)*.

28. As per **Claims 20 and 29**, but more specifically to Claim 20, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 19 wherein

the section is formed by at least one memory module *(as above, Koos, memory boards, column 1 lines 36-38)*.

29. As per **Claim 21**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 19 wherein

the addresses of the memory units located in the section with greatest size are firstly assigned, and the addresses of the memory units located in the section with smallest size are lastly assigned *(Hirschberg, section 3.1)*.

30. As per **Claim 22**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 19 wherein

the addresses of the memory units located in the section with grater size are smaller than the addresses of memory units located in the section with smaller size *(Hirschberg, section 3.1)*.

31. As per **Claims 23 and 30**, but more specifically to Claim 23, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 19 wherein

the bit-patterns are exclusive to each other *(invariant in Hirschberg, as otherwise the algorithm would not solve stated problem, section 3.1)*.

32. As per **Claims 24 and 31**, but more specifically to Claim 24, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 19 wherein

the bit-pattern is obtained by all the common bits of the address in each section *(see 103 rejection of Claim 19 above)*.

33. As per **Claims 25 and 32**, but more specifically to Claim 24, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 19 wherein

the bit-pattern is obtained by partial common bits of the address in each section (*see the rejection of Claims 25 and 32 under Patterson above, and the 103 rejection of Claim 14 above).*

34. As per **Claims 26 and 33**, but more specifically to Claim 26, Koos, Schmisseur and Hirschberg disclose The memory address decoding method of Claim 19 wherein

the given address is located in the objective section when certain bits of the given address completely match the bit-pattern of the objective section *(Hirschberg, section 3.1 and Schmisseur, column 4 lines 51-67).*

35. As per **Claim 14**, Koos, Schmisseur and Hirschberg disclose a control circuit of memory address decoding for

determining whether a given address *(Koos, memory address location, column 1 line 22)* is located in one of a plurality of sections *(Koos, memory boards, column 1 line 13)*, each section having a plurality of memory units and each memory unit having a unique corresponding address *(Koos, memory locations, column 1 line 18)*, the corresponding address using the binary system *(Koos, column 1 lines 39-44)*, the control circuit comprising:

an access module *(Koos, address bus 14, Figure 1)* for receiving the given address;

making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size *(Hirschberg, section 3.1 lines 1-2)*, and if the size of a first section is equal to the size of a second section, the first and the second sections are capable of being swapped

(Hirschberg discloses the elements being listed in order of non-increasing probability, which inherently does not render incapable the possibility of elements with the same probability being in any order, section 3.1, lines 1-2); and

a comparing module *(Koos, Figure 2)* for building a bit-pattern for each section based on its corresponding addresses *(Schmisseur, column 4 lines 55-59)* and sending a plurality of comparison signals after comparing the given address with those of each bit-pattern *(Koos, Figure 3)*.

Koos, Schmisseur and Hirschberg disclose using an algorithm *(Hirschberg, "Shannon-Fano coding", section 3.1)* for making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size, but do not disclose using a sorting module to do the same.

Koos, Schmisseur, Hirschberg and the concept of implementing algorithms as modules are analogous art in that Koos discloses using a module for comparing *(Koos, Figure 3)*. At the time of the invention it would have been obvious to one with ordinary skill in the art to implement the Shannon-Fano algorithm as taught by Hirschberg as a hardware sorting module.

The motivation would have been that the rest of Koos's system was implemented in hardware. Accordingly, implementing the Shannon-Fano algorithm in hardware would have not significantly modified the system architecture.

Therefore, it would have been obvious to implement the sorting algorithm taught by Koos, Schmisseur and Hirschberg as a hardware sorting module for the benefit of minimal modification to the system, to obtain the invention of Claim 14.

36. As per **Claim 15**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14 further comprising

a logic module *(Koos, element 30, Figure 2)* responsible for receiving the comparison signals and sending a decoding result to determine the given address is located in one of the sections *(Koos, board enable command 32, Figure 2)*.

37. As per **Claim 16**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14, wherein

the sections are a plurality of memory modules *(interpreted as per Claim 2, Koos, memory boards, column 1 lines 36-38)*.

38. As per **Claim 17**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14 wherein

the single bit-pattern is built for each section in the comparing module, the bit-pattern consisting of all common bits of the corresponding addresses in each section *(Schmisseur, column 4 lines 55-59)*.

VII. REJECTIONS BASED ON DOUBLE PATENTING

39. The following forms the basis for all non-statutory double patenting rejections set forth in this Office action:

> The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759

F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

40. **Claim 19** is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1-2, 4-5, 12-14 and 16 of copending Application No. 10/708103 in view of Schmisseur et al. *(US Patent Number 6,128,718)*. This is a **provisional** obviousness-type double patenting rejection.

41. The Examiner notes that though the inventive entities are different, the assignee for both applications is Via Technologies Inc.

42. Claim 19 of the instant application is compared to Claim 19 of the copending Application in the following table:

Instant Application	Copending Application
A memory address decoding method for determining an objective section of a given address in a memory, wherein the memory is formed by at least one section with at least one memory unit, the method comprising:	A memory address decoding method for determining an objective section of a given address in a memory, wherein the memory is formed by at least one section, which comprises at least one memory unit having a corresponding address, the method comprising:
assigning an address to each memory unit according to the memory size of the section;	
obtaining at least one bit-pattern of each section according to the common rules of the bit of the addresses;	obtaining at least one bit-pattern according to a common pattern of bits of the addresses;

comparing the given address with each bit-pattern to determine the objective section of the given address.	comparing the given address with each bit-pattern to determine the objective section of the given address.

43. The copending Application does not disclose assigning an address to each memory unit according to the memory size of the section.

Schmisseur discloses assigning an address to a memory unit according to the memory size of the section *(column 4 lines 51-67)*.

The copending Application and Schmisseur are analogous art in that they both deal with memory addressing methods. At the time of the invention it would have been obvious to modify the copending Application to use Schmisseur's address resizing.

The motivation for doing so would have been to allow address space sizes to be changed and behave as if the address space size was fixed *(Schmisseur, column 3 lines 33-36)*. This would allow the device to use whatever RAM devices are controlled by it *(column 2 lines 60-67)*.

Therefore, it would have been obvious to combine the copending Application and Schmisseur for the benefit of extensibility of memory, to obtain Claim 19 of the instant application.

IX. CLOSING COMMENTS

44. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

a. STATUS OF CLAIMS IN THE APPLICATION

45. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). SUBJECT MATTER CONSIDERED ALLOWABLE

46. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

47. The prior art of record neither anticipates nor renders obvious the below recited combinations:

a. The primary reasons for allowance of Claim 18 in the instant application is the combination with the inclusion that:

b. a plurality of comparing units, each comparing unit comprising: **a plurality of NXOR gates, each of the NXOR gates having two inputs for respectively receiving the output of one of the first-level AND gates and a standard address generated from the bit-patterns.**

a(2). CLAIMS NO LONGER IN THE APPLICATION

48. Claims 1-13 were cancelled by the amendment dated June 29, 2006.

a(3). CLAIMS REJECTED IN THE APPLICATION

49. Per the instant office action, Claims 14-17 and 19-33 have received a second action on the merits and are subject of a second action final.

b. DIRECTION OF FUTURE CORRESPONDENCES

50. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

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